Specification

Instantaneous Voltage Dip Detection Device

Technical Field

This invention relates to an instantaneous voltage dip detection device for detecting an instantaneous voltage dip in distribution network that occurs due to lightning or the like.

Background Art

As has been disclosed, for example, in the Japanese Patent Publication (unexamined) 2000-55947 and the Japanese Patent Publication (unexamined) 2002-171690 respectively, according to the publicly known instantaneous voltage dip detection devices, results of subtraction between an absolute value waveform of a reference sine wave and a reference cosine wave each synchronizing with a supply voltage and an absolute value waveform of a supply sine wave and a supply cosine wave are respectively obtained; the obtained results of subtraction are then integrated; and in the case where any of the results of integration exceeds a reference value, it is determined that a voltage dip has occurred.

In the aforementioned conventional system, however, since the integration is utilized for the detection of voltage dip, a problem exists in that it takes a time of about 1/4 cycle of an AC waveform in the detection and determination. Moreover, another problem exists in that if arranging an instantaneous voltage dip

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compensating device using such an instantaneous voltage dip detection device, service interruption over 1/4 cycle takes place from the start of voltage dip up to the switching to the voltage dip compensating operation.

Disclosure of Invention

This invention was made to solve the above-discussed problems and has an object of providing a system for detecting a voltage dip at a high speed.

To accomplish the foregoing object, an instantaneous voltage dip detection device according to this invention is characterized by including:

phase shifting means for shifting a supply voltage waveform by a predetermined angle and generating a phase shift voltage waveform;

phase lock means for detecting the zero voltage phase of the supply voltage waveform;

supply voltage waveform threshold generating means for generating a supply voltage waveform threshold acting as a voltage dip determination reference with respect to the mentioned supply voltage waveform in synchronization with the mentioned phase lock means;

phase shift voltage waveform threshold generating means for generating a phase shift voltage waveform threshold acting as a voltage dip determination reference with respect to the mentioned phase shift voltage waveform;

determination region setting means for setting a part or all of absolute values of the mentioned supply voltage waveform threshold and phase shift voltage

waveform threshold that are larger than a predetermined value as being a comparative determination effective region;

supply voltage waveform comparing means for outputting a voltage dip detection signal based on the comparison between the mentioned supply voltage waveform and the supply voltage waveform threshold, in the case where the mentioned determination region setting means determines as being a comparative determination effective region of the supply voltage waveform; and

phase shift voltage waveform comparing means for outputting a voltage dip detection signal based on the comparison between the mentioned phase shift voltage waveform and the phase shift voltage waveform threshold, in the case where the mentioned determination region setting means determines as being a comparative determination effective region of the phase shift voltage waveform.

Another instantaneous voltage dip detection device according to this invention is characterized by including:

phase lock means for detecting the zero voltage phase of the supply voltage waveform;

supply voltage waveform threshold generating means for generating a supply voltage waveform threshold acting as a voltage dip determination reference with respect to the mentioned supply voltage waveform in synchronization with the mentioned phase lock means;

waveform recording means for recording sequentially supply voltage waveforms in synchronization with the phase lock means;

recorded waveform threshold generating means for generating a lower limit threshold or an upper limit threshold by a predetermined calculation based on the mentioned recorded waveforms;

determination region setting means for setting a comparative determination effective region in synchronization with the phase lock means;

supply voltage waveform comparing means for outputting a voltage dip detection signal based on the comparison between the mentioned supply voltage waveform and the supply voltage waveform threshold, in the case where the mentioned determination region setting means determines as being a comparative determination effective region of the supply voltage waveform;

recorded waveform comparing means for outputting a voltage dip detection signal based on the comparison between the mentioned supply voltage waveform and the recorded waveform threshold, in the case where the mentioned determination region setting means determines as being a comparative determination effective region of the recorded waveform;

continuity determination means for determining that the mentioned supply voltage waveform comparing means outputs the voltage dip detection signal continuously for a predetermined time period;

logical multiplication (AND) means between the output of the supply voltage waveform comparing means and the output of the recorded waveform comparing means; and

voltage dip detection output means for outputting

a voltage dip detection signal by logical addition (OR) means between the output of the mentioned logical multiplication(AND) means and the output of the continuity determination means.

According to this invention, since the detection device not using any integration but using an instantaneous comparison is used for detection of a voltage dip, it is possible to detect voltage dip at a high speed. Further, since the detection device not using any integration taking a long time (over 1/4 cycle) is used for the detection of voltage dip, it is possible to detect voltage dip at a high speed. Switching a phase to be detected makes it possible to carry out a determination processing with a high level signal at all times, enabling to perform a stable detection. Further, carrying out an operation for a short time in a low-level signal region (near zero voltage phase) makes it possible to perform a stable detection. Furthermore, even in the state of superimposed harmonics, a stable detection can be performed by relieving the threshold conforming to a level of the harmonics and carrying out a comparative determination in comparison with the recorded waveforms.

Brief Description of Drawings

Fig. 1 is a block diagram showing an instantaneous voltage dip detection device according to Embodiment 1 of the present invention.

Fig. 2 is a waveform chart showing each of signal waveforms at the normal time of the instantaneous voltage dip detection device in Fig. 1.

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Fig. 3 is a signal waveform diagram showing each of signal waveforms at the time of occurrence of a voltage dip in the instantaneous voltage dip detection device in Fig. 1.

Fig. 4 is a block diagram showing an instantaneous voltage dip detection device according to Embodiment 2 of the invention.

Fig. 5 is a block diagram showing an instantaneous voltage dip detection device according to Embodiment 3 of the invention.

Fig. 6 is a block diagram showing phase shifting means of an instantaneous voltage dip detection device in detail according to Embodiment 5 of the invention.

Fig. 7 is a waveform diagram showing phase shift voltage waveforms according Embodiment 5 of the invention, and in which phase is inverted by 180 degree and harmonics are superimposed by 5 % using an all-pass filter.

Fig. 8 is a waveform diagram showing phase shift voltage waveforms according to a comparative example with Fig. 7, and in which phase is inverted by 180 degree and harmonics are superimposed by 5 % using differentiation circuit.

Fig. 9 is a waveform diagram showing transient waveforms at the time of occurrence of an instantaneous voltage dip of the phase shift means by the instantaneous voltage dip detection device in detail according to Embodiment 5 of the invention.

Fig. 10 is a block diagram showing an instantaneous voltage dip detection device according to Embodiment 10 of the invention.

Fig. 11 is a block diagram showing an instantaneous voltage dip detection device according to Embodiment 11 of the invention.

Best Mode for Carrying Out the Invention
Embodiment 1

Fig. 1 is a block diagram showing an instantaneous voltage dip detection device according to Embodiment 1 of the present invention, Fig. 2 is a waveform chart showing each of signal waveforms at the normal time of the instantaneous voltage dip detection device in Fig. 1, and Fig. 3 is a signal waveform diagram showing each of signal waveforms at the time of occurrence of a voltage dip in the instantaneous voltage dip detection device in Fig. 1.

Now Embodiment 1 is hereinafter described with reference to Figs. 1 to 3. The instantaneous voltage dip detection device shown in Fig. 1 includes: phase shift means 2 for shifting a phase of a supply voltage waveform 11 (see Fig. 2) being a signal waveform of a power supply 1 by a predetermined angle (for example 20° to 160°, more preferably 90°); and phase lock means 3 for detecting zero voltage phase (zero-cross point) of the supply voltage waveform. In synchronization with this phase lock means 3, power supply waveform threshold generating means 4 generates a power supply waveform threshold 12 (see Fig. 2) serving as a voltage dip criterion with respect to the supply voltage waveform 11. On the other hand, phase shift voltage waveform threshold generating means 5 generates a phase shift voltage waveform threshold 14

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(see Fig. 2) serving as a voltage dip determination criterion with respect to a phase shift voltage waveform 13 (see Fig. 2) shifted by about 90° from the zero voltage phase of the supply voltage waveform 11 detected by the phase lock means 3. In the mentioned process, the power supply waveform threshold generating means 4 and the phase shift voltage waveform threshold generating means 5 prepare the threshold 12 and the threshold 14 by multiplying data of table form, in which phase and amplitude value of a sine wave (trigonometric function) preliminarily stored in a memory are paired, by a set value set by user or manufacturer, and output them.

For example, in a manufacturing apparatus driven at a supply voltage of which effective value is 200V, when an input voltage has dipped to not higher than 160V, a set value is 0.8 (=160/200) in order to detect the instantaneous voltage dip. That is, the threshold 12 and the threshold 14 are prepared and outputted so that amplitude is 0 when phase is 0π (=200×$\sqrt{2}$×sin(0π)× 0.8), amplitude is $80\sqrt{2}$ when phase is $\pi/6$ (=200×$\sqrt{2}$ ×sin($\pi/6$)×0.8), amplitude is 160 when phase is $\pi/4$ (=200 ×$\sqrt{2}$×sin($\pi/4$)×0.8), and amplitude is $160\sqrt{2}$ when phase is $\pi/2$ (=200×$\sqrt{2}$×sin($\pi/2$)×0.8).

Determination region setting means 6 is provided to set, in synchronization with the phase lock means, a part of the supply voltage waveform threshold 12 and phase shift voltage waveform threshold 14 that are larger than a predetermined value, e.g., a part in which amplitude of each threshold is larger than about 70% of a peak value line 100 (sin($n\pi/4$)=0.707⋯, n=1, 3, 5, 7⋯), as being

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a comparative determination effective region. Further, supply voltage waveform comparing means 7 and phase shift voltage waveform comparing means 8 are provided. The supply voltage waveform comparing means 7 makes a comparison in magnitude between a supply voltage waveform 11 and a supply voltage waveform threshold 12 in the case where the determination region setting means 6 has determined a comparative determination region 70 (for example, $\pi/4$ to $3\pi/4$, $5\pi/4$ to $7\pi/4$ in Fig. 2) of the supply voltage waveform, and then outputs a voltage dip detection signal. The phase shift voltage waveform comparing means 8 makes a comparison in magnitude between a phase shift voltage waveform 13 and a phase shift voltage waveform threshold 14 in the case where the determination region setting means 6 has determined a comparative determination region 80 (for example, 0 to $\pi/4$, $3\pi/4$ to $5\pi/4$, $7\pi/4$ to 2π in Fig. 2) of the supply voltage waveform, and then outputs a voltage dip detection signal.

Furthermore, there are provided logical addition (OR) means 9 for outputting a logical addition (OR) of output of the supply voltage waveform comparing means 7 and output of the phase shift voltage waveform comparing means 8, and voltage dip signal detection output means 10 for outputting a voltage dip signal in the case where any voltage dip has been detected by the supply voltage waveform comparing means 7 or by the phase shift voltage waveform comparing means 8 upon receiving the output of the logical addition (OR) means 9.

Operations of the instantaneous voltage dip detection device according to Embodiment 1 arranged as

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described above are hereinafter described with reference to Figs. 1 to 3. As shown in Fig. 2, in the normal state that there is neither abnormality in supply voltage nor voltage dip, the supply voltage waveform comparing means 7 makes a comparison in magnitude between the supply voltage waveform 11 and supply voltage waveform threshold 12 of the power supply voltage 1 being in synchronization with each other by the phase lock means 3 in a region where the supply voltage waveform threshold 12 determined by the determination region setting means 6 is not smaller than a predetermined value, for example, at the phases of $\pi/4$ to $3\pi/4$ and $5\pi/4$ to $7\pi/4$ (in repeating fashion) of Fig. 2 being a region 70 in which magnitude of the threshold is not smaller than 70% of the peak value.

Further, the phase shift voltage waveform comparing means 8 makes a comparison in magnitude between the phase shift voltage waveform 13 and phase shift voltage waveform threshold 14 being in synchronization with each other in a region where the phase shift voltage waveform threshold 14 determined by the determination region setting means 6 is not smaller than a predetermined value, for example, at the phases of 0 to $\pi/4$, $3\pi/4$ to $5\pi/4$ and $7\pi/4$ to 2π (in repeating fashion) of Fig. 2 being a region 80 in which magnitude of the threshold is not smaller than 70% of the peak value.

As shown in Fig. 3, in the case where an instantaneous voltage dip occurs at the phase $\pi/2$ in the supply voltage 1, the supply voltage waveform comparing means 7 that compares amplitude in absolute value of the supply voltage waveform 11 and the supply voltage waveform threshold

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12 has a smaller supply voltage waveform 11 than the supply voltage waveform threshold 12, and therefore outputs an instantaneous voltage dip signal. When it is determined that such an instantaneous voltage dip has occurred (i.e., as the phase is on the positive side, in the case where the supply voltage waveform 11 is less than the supply voltage waveform threshold 12), a signal is outputted from the logical addition (OR) means 9, and a voltage dip detection signal is outputted from the voltage dip detection signal output means 10.

As described above, since the supply voltage waveform comparing means 7 determines the instantaneous voltage dip continuously at an instantaneous value, any instantaneous voltage dip can be detected at a high speed, for example, at a cycle of not more than 1/10 of one wavelength. Further, since the voltage dip can be determined using only a region where voltage waveform level for detecting the voltage dip is larger, stable and constant detection can be performed. Accordingly, when arranging a voltage compensation apparatus in combination of the instantaneous voltage dip detection device, it becomes possible to compensate an instantaneous voltage dip in a very short time.

Further, since a phase shift voltage waveform shifting a supply voltage waveform by 90° is also utilized in the detection of the instantaneous voltage dip, the instantaneous voltage dip detection device can be used for detecting any region, where voltage waveform level is large, of at least either the supply voltage waveform or the phase shift voltage waveform, and a determination

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region that is continuous in time can be obtained.

In addition, although an example in which phase shift voltage waveform is one is described above, it is possible that there are two or more phase shift voltage waveforms. For example, in the case of two phase shift voltage waveforms, phase is shifted by every 60°. In this case, however, circuit arrangement will be complicated and therefore one phase shift voltage waveform is preferably.

Embodiment 2.

Fig. 4 is a block diagram showing an instantaneous voltage dip detection device according to Embodiment 2 of the invention. In this Embodiment 2, second phase lock means 15 is provided for detecting zero voltage phase (zero-cross point) of the phase shift voltage waveform 13. The phase shift voltage waveform threshold generating means 5 generates, in synchronization with the second phase lock means 15, a phase shift voltage waveform threshold 14 serving as a voltage dip determination criterion with respect to the phase shift voltage waveform 13. The remaining part is arranged in the same manner as in Fig. 1, and the same reference numerals are designated to the same elements omitting further description.

In this Embodiment 2, even if there is any variation in phase shift amount of the phase shift means 2, since a threshold is generated by the phase shift voltage waveform threshold generating means 5 on the basis of zero voltage phase of the output voltage waveform of the phase shift means 2, the variation in phase shift amount

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can be compensated, and stable and constant detection
can be performed.

Embodiment 3.

Fig. 5 is a block diagram showing an instantaneous
voltage dip detection device according to Embodiment 3
of the invention. In this Embodiment 3, phase difference
detection means 16 is provided. The phase difference
detection means 16 detects zero voltage phase of the
phase shift voltage waveform 13, and a difference from
zero voltage phase (zero-cross point) of the supply
voltage waveform 11 obtained from the phase lock means
3 is obtained. The phase shift voltage waveform threshold
generating means 5 generates, in synchronization with
the phase difference detection means 16, a phase shift
voltage waveform threshold 14 serving as a voltage dip
determination criterion with respect to the phase shift
voltage waveform 13. The remaining part is arranged in
the same manner as in Fig. 1, and the same reference
numerals are designated to the same elements omitting
further description.

In this Embodiment 3, even if there is any variation
in phase shift amount of the phase shift means 2, a phase
difference from the phase lock means 3 is detected by
the phase difference detection means 16 and a phase of
the threshold generated by the phase shift voltage
waveform threshold generating means 5 is controlled by
the output thereof. Therefore, even if there is any
variation in phase shift amount of the phase shift means
2, the variation in phase shift amount can be compensated,

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and stable and constant detection can be performed.

Embodiment 4.

In this embodiment, referring to the arrangements shown in Figs. 1, 4 and 5, the supply voltage waveform comparing means 7 and the phase shift voltage waveform comparing means 8 have a counter function not shown, and a voltage dip detection signal is generated only when it is determined that a voltage dip is generated continuously for a predetermined time set in the counter function. Malfunction due to noise can be effectively prevented. It is preferable that the counter function is provided with the logic addition (OR) means 9.

Embodiment 5.

Fig. 6 is a block diagram showing in detail phase shifting means employed in an instantaneous voltage dip detection device according to Embodiment 5 of the invention. The phase shift means 2 is an all-pass filter consisting of resistors 17, 18, 19, a capacitor 20 and an amplifier 21. Shifting operation is determined depending on a value (time constant CR) between the resistor 18 (constant R) and the capacitor 20 (constant C). In order to set a shift angle to be within a range of 20° to 160°, the circuit constant value $1/(2\pi CR)$ is set to be within a range of 8 to 340. Each of the resistors and the capacitor is set to a value for phase shifting the supply voltage waveform 11 of which supply voltage cycle is 55Hz by about 90°, for example.

Generally, a differentiation circuit is sometimes

employed as a method of phase shifting a waveform by 90° ..
However, in the case of using a differentiation circuit,
a gain of high frequency component contained in the supply
voltage waveform becomes large, and a waveform of which
out of alignment is large and which is not suitable for
the voltage dip detection is outputted (for example, see
a phase shift voltage waveform 13b at the time of
superimposition of harmonics shown in Fig. 8). To
suppress this variation in waveform, it may be an idea
to combine a low-pass filter circuit. In this case,
however, a problem exists in that the low-pass filter
may extinguish the sharp variation of the waveform
generated at the time of voltage dip, thereby taking much
time in the detection.

According to this Embodiment 5, since an all-pass
filter consisting of resistors, capacitor and amplifier
is used as phase shift means, it becomes possible to
establish the supply voltage waveform 11 and the gain
of the phase shift voltage waveform 13 after the phase
shifting by about 90° to be almost equal. There is no
need of reducing such a gain by combining a low-pass filter
circuit to eliminate the high frequency component as is
required in the case of using a differentiation circuit.
Thus, an advantage exists in that a phase shift waveform
can be generated with a simple circuit arrangement.

Embodiment 6.

This embodiment shows an example of circuit
arrangement of Fig. 5 in which the phase shift means 2
including an all-pass filter of Fig. 6 is used. Fig. 7

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shows a phase shift voltage waveform 13a in which third harmonic (of which phase is inverted by 180 degree) is superimposed by 5 % using an all-pass filter as phase shift means as shown in Fig. 5. Fig. 8 shows, as a comparative example, a phase shift voltage waveform 13b in which third harmonic (of which phase is inverted by 180 degree) is superimposed by 5 % using a differentiation circuit as phase shift means. For reasons of convenience, the threshold 12a and threshold 14a are the same as in Fig. 7.

In this Embodiment, the phase difference detection means 16 of Fig. 5 has a recording function and harmonics level determination function.

Referring to Fig. 7, by detecting a difference (phase shift) between a phase value in the mentioned recording function that records a zero voltage phase of the phase shift voltage waveform 13 at the normal time when no harmonics are superimposed on the supply voltage and a zero voltage phase of the phase shift voltage waveform 13a, the mentioned harmonics level determination function determines a level of harmonics. By a command of the harmonics level determination function, the phase shift voltage waveform threshold generating means 5 generates a threshold 14a that is reduced by 2% as compared with the normal time. For example, supposing that a threshold when harmonics are zero is $160\sqrt{2}$, the threshold 14a when the harmonics are superimposed by 5% is $157\sqrt{2}(160 \times 0.98\sqrt{2})$.

Specifically, in the case of using an all-pass filter shown in Fig. 6, due to circuit arrangement thereof, when

the harmonics are superimposed, although the absolute value of the voltage waveform 13a after the phase shift is almost the same as that of the normal time phase shift voltage waveform 13, there arises a phase shift 90. Utilizing this phenomenon, level of the harmonics are detected. On the other hand, as shown in Fig. 8, in the case of using a differentiation circuit, due to circuit arrangement thereof, when the harmonics are superimposed, although there arises substantially no phase shift, the absolute value of the voltage waveform 13a after the phase shift has a large variation in waveform thereof as compared with that of the normal time phase shift voltage waveform 13.

Therefore accuracy in the detection of instantaneous voltage dip is lowered as compared with that in Fig. 7.

According to Embodiment 6 of the invention, even in the case of superimposing the harmonics on the supply voltage, level of the harmonics are detected and threshold is reduced, thereby making it possible to perform a stable detection of voltage dip.

Embodiment 7.

This embodiment relates to an instantaneous voltage dip detection device of which circuit arrangement is based on Figs. 1, 4 and 5. In this Embodiment 7, the power supply waveform threshold generating means 4 and the phase shift voltage waveform threshold generating means 5 have a waveform recording function. Referring to Fig. 4, this waveform recording function records sequentially the supply voltage waveform 11 or the phase shift voltage

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waveform 13 in synchronization with the phase lock means 3 or the second phase lock means 15.

A predetermined value, for example, 20% of a recorded value is added to or subtracted from the recorded supply voltage waveform 11 or phase shift voltage waveform 13 to obtain an upper limit threshold and a lower limit threshold. For example, a value of which waveform is shifted by ±20% with respect to the previous waveform is established as an upper limit threshold and a lower limit threshold.

The supply voltage waveform comparing means 7 and phase shift voltage waveform comparing means 8 determines that an instantaneous voltage dip has occurred when the supply voltage waveform 11 or phase shift voltage waveform 13 varies over the mentioned upper limit threshold and the lower limit threshold.

In this manner, an advantage is obtained such that even under the condition that determination of a threshold is difficult, it is possible to perform a stable detection of voltage dip. Although 20% is taken as a predetermined value is in the foregoing description, the percentage can be changed depending upon the phase.

Embodiment 8.

This embodiment relates to an instantaneous voltage dip detection device of the circuit arrangement shown in Fig. 5. Fig. 9 shows a transient waveform at the time of generating an instantaneous voltage dip of the phase shift means 2 according to the foregoing Embodiment 5 of the invention.

In the phase shift means 2 according to Embodiment 5 (see Fig. 6), when occurring a sharp instantaneous voltage dip at a predetermined phase, for example, at $3\pi/4$ to π, a transient phenomenon 120 of the phase shift voltage waveform is generated, in which phase shift voltage waveform 13 swings in the opposite direction of the phase shift voltage waveform threshold 14 (voltage rising direction, i.e., positive direction).

At this predetermined phase, the phase shift voltage waveform threshold generating means 5 generates not only a determination threshold of voltage dip but also a determination threshold of voltage rising, and the phase shift voltage waveform comparing means 8 determines the voltage dip based on both of the mentioned thresholds. In the case of a sharp change in voltage, the determination is carried out based on the voltage rising threshold and in the case of a slow change in voltage, the determination is carried out based on the voltage dip threshold.

According to this Embodiment 8, an advantage is obtained such that it is possible to perform a speedy detection of instantaneous voltage dip over a wide range of phase.

Embodiment 9.

This embodiment relates to an instantaneous voltage dip detection device of the circuit arrangement shown in Fig. 5. In this Embodiment 9, phase shift voltage waveform threshold generating means 5 have a waveform recording function. This waveform recording function records sequentially the phase shift voltage waveform

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13 in synchronization with the phase difference detection means 16.

At a voltage dip determination threshold and at a predetermined phase, for example, at $3\pi/4$ to π, the phase shift voltage waveform threshold generating means 5 determines a voltage rising determination threshold by adding or subtracting a predetermined value to or from a recorded waveform value of the recorded phase shift voltage waveform 13, for example, 20% of the value. The phase shift voltage waveform comparing means 8 determines a voltage dip based on the mentioned both thresholds. In the case of a sharp change in voltage, the determination is carried out based on the voltage rising threshold and in the case of a slow change in voltage, the determination is carried out based on the voltage dip threshold. Although 20% is taken as a predetermined value is in the foregoing description, the percentage can be changed depending upon the phase.

According to this Embodiment 9, an advantage is obtained such that it is possible to perform a speedy detection of instantaneous voltage dip over a wide range of phase.

Embodiment 10.

Fig. 10 is a block diagram showing an instantaneous voltage dip detection device according to Embodiment 10 of the invention.

In this Embodiment 10, a phase lock means 3 is provided for detecting zero voltage phase(zero-cross point) of the supply voltage waveform 11 which is a signal

waveform of the supply voltage 1. In synchronization with an output of this phase lock means 3, the supply voltage waveform threshold generating means 4 generates the supply voltage waveform threshold 12 acting as a voltage dip determination reference with respect to the supply voltage waveform 11.

The supply voltage waveform comparing means 7 determines that an instantaneous voltage dip has occurred, in the case where the supply voltage waveform 11 is below the supply voltage waveform threshold (i.e., goes down beyond the threshold in the direction of AC zero voltage) in a region where the determination region setting means 6 has determined a comparative determination effective region (for example, $\pi/10$ to $9\pi/10$, $11\pi/10$ to $19\pi/10$).

Waveform recording means 22 records sequentially the supply voltage waveform in synchronization with the phase lock means 3, and recorded waveform threshold generating means 23 establishes an upper limit threshold and a lower limit threshold by adding and/or subtracting a predetermined value, for example, 20% based on a recorded waveform value of the recorded supply voltage waveform. For example, a value of which waveform is shifted by $\pm$ 20% with respect to the previous waveform is established as an upper limit threshold and a lower limit threshold. a value of which waveform is shifted by $\pm 20\%$ with respect to the previous waveform. Although the same value is taken as a predetermined value over the all phase region in the foregoing description, any value different depending upon the phase can be set.

Recorded waveform comparing means 24 determines that

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an instantaneous voltage dip has occurred in the case where the supply voltage waveform 11 has changed over the mentioned upper limit threshold and lower limit threshold in a region where the mentioned determination region setting means 6 determines as being a comparative determination effective region.   In   this   regard, although both upper limit threshold and lower limit threshold are used, it is preferable to use only the lower limit threshold.

Continuity determination means 25 determines that a voltage dip in which voltage is reduced gently has occurred in the case where the supply voltage waveform comparing means 7 has determined occurrence of an instantaneous   voltage   dip   continuously   for   a predetermined time period (for example, for 1/4 cycle).

Logical multiplication (AND) means 26 determines that an instantaneous voltage dip has occurred in the case where both recorded waveform comparing means 24 and supply voltage waveform comparing means 7 have determined occurrence of an instantaneous voltage dip.   Thus, an advantage is such that even in the case where high harmonics are mixed at a high level and occurrence of an instantaneous voltage dip is erroneously determined in the voltage waveform comparison, the recorded waveform comparing means 24 determines the voltage dip rightly, enabling to perform a stable voltage dip detection.   In the case of very gentle voltage reduction, there may be a case where a difference between the current waveform and the waveform preceding by 1 cycle is so small that the recorded waveform comparing means 24 cannot determine the voltage

dip. Even in such a case, the continuity determination means 25 can detect the voltage dip.

Logical addition (OR) means 27 determines that an instantaneous voltage dip has occurred when either the logical multiplication (AND) means 26 or the continuity determination means 25 has determined occurrence of an instantaneous voltage dip.

As a result, even in the case where harmonics are mixed at a high level and an instantaneous voltage dip of gentle voltage has occurred, it is possible to perform a stable detection.

Embodiment 11.

Fig. 11 is a block diagram showing an instantaneous voltage dip detection device according to Embodiment 11 of the invention.

In this Embodiment 11, a phase lock means 3 is provided for detecting zero voltage phase(zero-cross point) of the supply voltage waveform 11 that is a signal waveform of the supply voltage 1. In synchronization with an output of this phase lock means 3, the supply voltage waveform threshold generating means 4 generates the supply voltage waveform threshold 12 acting as a voltage dip determination reference with respect to the supply voltage waveform 11.

The supply voltage waveform comparing means 7 determines that an instantaneous voltage dip has occurred, in the case where the supply voltage waveform 11 is below the supply voltage waveform threshold (i.e., goes down beyond the threshold in the direction of AC zero voltage)

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in a region where the determination region setting means 6 has determined a comparative determination effective region (for example, $\pi/10$ to $9\pi/10$, $11\pi/10$ to $19\pi/10$).

Waveform recording means 22 records sequentially the supply voltage waveform in synchronization with the phase lock means 3, and recorded waveform threshold generating means 23 establishes an upper limit threshold and a lower limit threshold by adding and/or subtracting a predetermined value, for example, 20% based on a recorded waveform value of the recorded supply voltage waveform. For example, a value of which waveform is shifted by $\pm$ 20% with respect to the previous waveform is established as an upper limit threshold and a lower limit threshold. Although the same value is taken as a predetermined value over the all phase region in the foregoing description, any value different depending upon the phase can be set.

Recorded waveform comparing means 24 determines that an instantaneous voltage dip has occurred in the case where the supply voltage waveform 11 has changed over the mentioned upper limit threshold and lower limit threshold in a region where the mentioned determination region setting means 6 determines as being a comparative determination effective region. In this regard, although both upper limit threshold and lower limit threshold are used, it is preferable to use only the lower limit threshold.

Continuity determination means 25 determines that a voltage dip in which voltage is reduced gently has occurred in the case where the supply voltage waveform comparing means 7 has determined occurrence of an

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instantaneous voltage dip continuously for a predetermined time period (for example, for 1/4 cycle).

Waveform integrating means 28, in synchronization with the phase lock means 3, integrates and outputs a predetermined calculation value (for example, absolute value) of the supply voltage waveform 11 during the phase of 0 to $\pi/10$, $9\pi/10$ to π, $19\pi/10$ to 2π being near zero voltage phase.

Integrated threshold generating means 29 generates an integrated value during the mentioned phase (in this case 0 to $\pi/10$, $9\pi/10$ to π, $19\pi/10$ to 2π) of sine wave of a voltage value detected as an instantaneous voltage dip, the integrated value being an integration waveform threshold serving as a voltage dip determination reference. The integration waveform threshold is preferably selected so that noise detection sensitivity is low as compared with the recorded waveform threshold from the viewpoint of preventing malfunction due to noise because there are much noise components in the region near zero voltage phase. For example, it is preferable that the integrated waveform threshold is established to be a value that is 50% of a value of an ideal waveform or previous waveform.

Integrated value comparing means 30 determines that an instantaneous voltage dip has occurred in the case that an output of the waveform integrating means 28 is below the integrated waveform threshold (i.e., goes down beyond the threshold in the direction of AC zero voltage) in a region where the determination region setting means 6 has determined a comparative determination effective

region (in this case, 0 to $\pi/10$, $9\pi/10$ to π, $19\pi/10$ to 2π).

Logical addition (OR) means 31 determines that an instantaneous voltage dip has occurred when either the voltage waveform comparing means 7 or the integrated value comparing means 30 has determined occurrence of an instantaneous voltage dip.

The logical multiplication (AND) means 26 determines that an instantaneous voltage dip has occurred in the case where both recorded waveform comparing means 24 and logical addition (OR) means 31 have determined occurrence of an instantaneous voltage dip.

In the region near zero voltage phase , influence of noise can re reduced by integration, enabling to perform stable voltage dip detection. Furthermore, an advantage is such that even in the case where harmonics are mixed at a high level and occurrence of an instantaneous voltage dip is erroneously determined in the voltage waveform comparison, the recorded waveform comparing means 24 determines the voltage dip rightly, enabling to perform a stable voltage dip detection. In the case of very gentle voltage reduction, there may be a case where a difference between the current waveform and the waveform preceding by 1 cycle is so small that the recorded waveform comparing means 24 cannot determine the voltage dip. Even in such a case, the continuity determination means 25 can detect the voltage dip.

Logical addition (OR) means 27 determines that an instantaneous voltage dip has occurred when either the logical multiplication (AND) means 26 or the continuity

determination means 25 has determined occurrence of an instantaneous voltage dip.

As a result, even in the case where harmonics are mixed at a high level and an instantaneous voltage dip of gentle voltage has occurred, it is possible to perform a stable detection.

Industrial Applicability

The present invention enables a voltage dip to be detected at a high speed, and is effective for detection of instantaneous voltage dip in distribution network occurring due to lightning.